Amendments to the Specification:

Please replace paragraph [0019] with the following amended paragraph:

[0019] FIG. 4 illustrates a second embodiment of a driver circuit 400 that may be used to implement the method 100 or 200. The driver circuit 400 comprises first and second switching circuits 402, 404, each of which is controlled by an input signal received at node IN. By way of example, the switching circuits 402, 404 may form an inverting ~~complimentary~~complementary metal-oxide semiconductor (CMOS) buffer 406 (i.e., with the first switching circuit taking the form of a p-channel field effect transistor (PFET), and with the second switching circuit taking the form of an n-channel field effect transistor (NFET)). The PFET is coupled via its source and drain between an output of the driver circuit (NODE_0) and a first intermediate node (BNP_UP). The NFET is coupled via its source and drain between NODE_0 and a second intermediate node (BNP_DN). The gates of the two FETs are coupled to each other at node IN, which is configured to receive an input signal.